What is claimed is:

1. A voltage reference generator for a hysteresis circuit, comprising:

- a first originator circuit to generate a first reference voltage;

- a second originator circuit to generate a second reference voltage;

- a selector circuit, coupled to the first and second originator circuits, to select one of the first and second reference voltages to be an output reference voltage based upon an output signal to the hysteresis circuit undertaking a high-to-low or low-to-high signal transition respectively;

- the first originator circuit including a first plurality of channel devices selected from either p-channel devices or n-channel devices; and

- the second originator circuit including a second plurality of channel devices selected from the other one of the p-channel devices and the n-channel devices.

2. The voltage reference generator of claim 1, wherein the first plurality of channel devices includes the p-channel devices and the second plurality of channel devices includes the n-channel devices.

3. The voltage reference generator of claim 1, wherein the first plurality of channel devices includes a first, a second, and a third p-channel device and wherein the second plurality of channel devices includes a first, a second, and a third n-channel device.

4. The voltage reference generator of claim 2, wherein the reference voltage generator includes a supply voltage and a ground; each of the channel devices has a source, a drain and a gate; the first originator circuit includes a first reference voltage node having the first reference voltage; the sources of the first and second p-channel devices are coupled to the source voltage and the drains of the first and second p-channel devices are coupled to the first reference voltage node; the source of the third p-channel device is coupled to the first reference voltage node and the drain of the third p-channel device is coupled to the ground; the gate of the first p-channel device is coupled to the first reference voltage node; and the gates of the second and third p-channel devices are coupled to the ground.

5. The voltage reference generator of claim 4, wherein the second originator circuit including a second reference voltage node having the second reference voltage; the drains of the first and second n-channel devices are coupled to the second reference voltage node and the sources of the first and second n-channel devices are coupled to the ground; the drain of the third n-channel device is coupled to the supply voltage and the source of the third n-channel device is coupled to the second reference voltage node; the gates of the second and third n-channel devices are coupled the supply voltage; and the gate of the first n-channel device is coupled to the second reference voltage node.

6. The voltage reference generator of claim 5, wherein the selector circuit is coupled between the first and second reference voltage nodes.

7. The voltage reference generator of claim 5, wherein the reference voltage generator includes an output reference voltage node having the output reference voltage; and the selector circuit includes a fourth p-channel device and a fourth n-channel device; the fourth p-channel device has the drain coupled to the output voltage reference node and the source coupled to the first reference voltage node and the fourth n-channel device has the drain coupled to the output voltage reference node and the source coupled to the second reference voltage node.

8. A hysteresis circuit, comprising:

- a sensing amplifier to generate an output signal having an output and two inputs with one of the inputs coupled to an input signal;

- a reference generator coupled to the output and the other one of the inputs of the sensing amplifier and responsive to the output signal to generate an output reference voltage;

- the reference generator including a first originator circuit to generate a first reference voltage; a second originator circuit to generate a second reference voltage; a selector circuit coupled to the first and second originator circuits to provide as the output

reference voltage either the first or second reference voltages based upon the output signal undertaking a falling signal transition or a rising signal transition respectively;

- the first originator circuit including a first one of a plurality of p-channel devices or n-channel devices; and

- the second originator circuit including the non-first one of the plurality of p-channel devices or n-channel devices.

9. The hysteresis circuit of claim 8, wherein the first originator circuit includes the plurality of p-channel devices and the second originator circuit includes a plurality of n-channel devices.

10. The hysteresis circuit of claim 8, wherein the first originator circuit includes a first, a second, and a third p-channel device and wherein the second originator circuit includes a first, a second, and a third n-channel device.

11. The hysteresis circuit of claim 10, wherein the reference voltage generator includes a supply voltage and a ground; each of the channel devices has a source, a drain and a gate; the first originator circuit includes a first reference voltage node having the first reference voltage; the sources of the first and second p-channel devices are coupled to the source voltage and the drains of the first and second p-channel devices are coupled to the first reference voltage node; the source of the third p-channel device is coupled to the first reference voltage node and the drain of the third p-channel device is coupled to the ground; the gate of the first p-channel device is coupled to the first reference voltage node; and the gates of the second and third p-channel devices are coupled to the ground.

12. The hysteresis circuit of claim 11, wherein the second originator circuit including a second reference voltage node having the second reference voltage; the drains of the first and second n-channel devices are coupled to the second reference voltage node and the sources of the first and second n-channel devices are coupled to the ground; the drain of the third n-channel device is coupled to the supply voltage and the source of the third n-channel device is coupled to the second reference voltage node; the gates of the second

and third n-channel devices are coupled the supply voltage; and the gate of the first n-channel device is coupled to the second reference voltage node.

13. The hysteresis circuit of claim 12, wherein the selector circuit is coupled between the first and second reference voltage nodes.

14. The hysteresis circuit of claim 12, wherein the reference voltage generator includes an output reference voltage node having the output reference voltage; and the selector circuit includes a fourth p-channel device and a fourth n-channel device; the fourth p-channel device has the drain coupled to the output voltage reference node and the source coupled to the first reference voltage node and the fourth n-channel device has the drain coupled to the output voltage reference node and the source coupled to the second reference voltage node.

15. The hysteresis circuit of claim 8, wherein the hysteresis circuit is included in an integrated circuit.

16. The hysteresis circuit of claim 15, wherein the integrated circuit is a microprocessor.

17. A system, comprising:

- an integrated circuit having a reference generator to generate an output reference voltage; a hysteresis circuit responsive to an input signal and the output reference voltage to generate an output signal; the reference generator including a first originator circuit to generate a first reference voltage; a second originator circuit to generate a second reference voltage; a selector circuit coupled to the first and second originator circuits to provide as the output reference voltage either the first or second reference voltages based upon the output signal undertaking a falling signal transition or a rising signal transition respectively; the first originator circuit including a first one of a plurality of p-channel devices or n-channel devices; and the second originator circuit including the non-first one of the plurality of p-channel devices or n-channel devices;

- a DRAM coupled to the integrated circuit; and

- an input/output interface coupled to the integrated circuit.

18. The system according to claim 17, the integrated circuit further includes a central processing unit, a main memory coupled to the central processor unit and at least one input/output module coupled to the central processor unit and the main memory.

19. The system of claim 17, wherein the first originator circuit includes the plurality of p-channel devices and the second originator circuit includes a plurality of n-channel devices.

20. The system of claim 17, wherein the first originator circuit includes a first, a second, and a third p-channel device and wherein the second originator circuit includes a first, a second, and a third n-channel device.

21. The system of claim 20, wherein the reference voltage generator includes a supply voltage and a ground; each of the channel devices has a source, a drain and a gate; the first originator circuit includes a first reference voltage node having the first reference voltage; the sources of the first and second p-channel devices are coupled to the source voltage and the drains of the first and second p-channel devices are coupled to the first reference voltage node; the source of the third p-channel device is coupled to the first reference voltage node and the drain of the third p-channel device is coupled to the ground; the gate of the first p-channel device is coupled to the first reference voltage node; and the gates of the second and third p-channel devices are coupled to the ground.

22. The system of claim 21, wherein the second originator circuit including a second reference voltage node having the second reference voltage; the drains of the first and second n-channel devices are coupled to the second reference voltage node and the sources of the first and second n-channel devices are coupled to the ground; the drain of the third n-channel device is coupled to the supply voltage and the source of the third n-channel device is coupled to the second reference voltage node; the gates of the second and third n-channel devices are coupled the supply voltage; and the gate of the first n-channel device is coupled to the second reference voltage node.

23. The system of claim 20, wherein the selector circuit is coupled between the first and second reference voltage nodes.

24. The system of claim 20, wherein the reference voltage generator includes an output reference voltage node having the output reference voltage; and the selector circuit includes a fourth p-channel device and a fourth n-channel device; the fourth p-channel device has the drain coupled to the output voltage reference node and the source coupled to the first reference voltage node and the fourth n-channel device has the drain coupled to the output voltage reference node and the source coupled to the second reference voltage node.

25. The system of claim 17, wherein the integrated circuit is a microprocessor.

26. The system of claim 17, wherein the input/output interface comprises a networking interface.

27. The system of claim 17, wherein the system is a selected one of a set-top box, an entertainment unit and a DVD player.